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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2187	28

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/205,086	BOGIN ET AL.	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 38-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28 and 38-49* is/are rejected.

7)☒ Claim(s) *5 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 and 38-49 are presented for examination.

SPECIFICATION

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. The following claims are objected to because:

the amendment to claim 5 has not been properly submitted. Is this claim dependent upon claim 3 or claim 4?

Claim 14 must end in a period.

35 USC § 112, 2nd paragraph

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 4-13 and 38-49 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4 and 38 have the language 'a clock generator to generate clock signals to generate clock signals to' which appears to either be redundant and confusing or clock signals are generating clock signals. Neither of these interpretations give a clear and concise meaning to the claim language.

Claims 5-13 and 39-49 are rejected as having the same deficiencies as the claim upon which they depend.

35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by **Direct Rambus™ Technology Disclosure**.

8. The **Direct Rambus™ Technology Disclosure** teaches the invention (claim 1) as claimed including a computer system comprising:

a memory which is taught as RDRAMs (e.g., see Figure 2 and the Introductions, page 4); and,

a memory controller having a refresh timing circuit to compensate for operating conditions in the computer system by evaluating time between memory refresh events when the computer system is operating in a normal mode as the refreshes performed to maintain data integrity of the memory when the system is not in the low power mode (e.g., see Figure 4 which show V_{ref}). The RDRAM has a self-refresh mode for when the system is in a low power state. The normal mode is specifically taught as the active mode which has a higher power consumption than the other modes of operations (e.g., see the second titled Power Management on page 13). The memory controller compensates for operating conditions in the computer system by having refresh capability, thereby having refresh timing circuitry, as there is a self-

refresh for the low power system operation which is different from the normal or active operating mode which must also have the RDRAM refreshed.

As to claim 2, the **Direct Rambus™ Technology Disclosure** teaches the refresh timing circuit triggers memory refresh events whenever the computer system is operating in a low power mode, the memory refresh events triggered based upon the evaluated time between memory refresh events when the computer system was operating in a normal mode as a self-refresh function which is used for low power applications (e.g., see the first paragraph of the second column on page 13).

As to claim 3, the **Direct Rambus™ Technology Disclosure** teaches the refresh timing circuit further comprises the following:

a clock generator to generate the clock pulses (e.g., see the section titled **Clocking** on page 9);

a first counter coupled to the clock generator to count the number of clock pulses between memory refresh events is taught inherently as being a necessary element used for refresh events, the memory must be refreshed on a periodic basis or time frame, this time frame must be detected or tracked and the method of doing this functionality is counting the clock pulses to determine the time since the last refresh event, the counter is incremented until a comparison with a predetermined number of clock pulses indicates a refresh must be performed (e.g., see the section titled **Clocking** on page 9 and the section titled **Features of the Rambus Memory Controller** on pages 14-15); and,

a storage register coupled to the clock generator and the counter to store a value representing the number of clock pulses between memory refresh events and a comparator coupled to the clock generator, the counter and the storage register as the memory controller

clearly supporting the necessary refresh function required for dynamic random access memory, different types of DRAM or RDRAM have different time requirements for when the memory must be refreshed to maintain the data integrity, to perform the refresh function the memory controller must store the predetermined value indicating when the refresh must be performed, the memory controller compares the number of clock pulses which have occurred since the last refresh operation to the predetermined number of clock pulses, when these values match the refresh is executed, given the details of the reference, this is the method and elements which one of ordinary skill in the art would know to be the method and elements used in the refreshing of the reference (e.g., see the section titled **Features of the Rambus Memory Controller** on pages 14-15).

As to claim 4, the **Direct Rambus™ Technology Disclosure** teaches the clock generator comprises:

a host clock refresh counter to reference a host clock signal to generate memory refresh events whenever the computer system is operating in a normal mode as the system using an external clock generator for the external clock signals as opposed to the internal clock generator (e.g., see Figure 4 on page 8); and,

a clock generator to generate clock signals to trigger the memory refresh events when the computer system is operating in the low power mode (e.g., see the section titled **DRAM Core Options** on pages 12-13, specifically the last paragraph of the section).

As to claim 5, the **Direct Rambus™ Technology Disclosure** used as 35 USC §102(b) art is still applied as given in the previous rejection, (the final office action, paper # 13 and repeated in the examiner's answer, paper # 19), this rejection for this non-amended claim was affirmed by the Board of Patent Appeals and Interferences and is now applied *res judicata*.

As to claim 15, **Direct Rambus™ Technology Disclosure** teaches the memory is an Extended Data Out Dynamic Random Access Memory, EDO RAM, and the memory controller would be an EDO RAM controller as one of ordinary skill in the art would know to match the controller with the type of memory used (e.g., see the table on page 5). Additionally, both types of memory can be used for low power modes.

9. The **Direct Rambus™ Technology Disclosure** teaches the invention (claim 16) as claimed including a memory controller comprising:

a refresh timing circuit to compensate for operating conditions in a computer system by evaluating time between memory refresh events when the computer system is operating in a normal mode as the refreshes used to maintain data integrity of the memory when the system is not in the low power mode (e.g., see Figure 4 which show V_{ref}). The RDRAM has a self-refresh mode for when the system is in a low power state. The normal mode is specifically taught as the active mode which has a higher power consumption than the other modes of operations (e.g., see the second titled Power Management on page 13). The memory controller compensates for operating conditions in the computer system by having refresh capability, thereby having refresh timing circuitry, as there is a self-refresh for the low power system operation which is different from the normal or active operating mode which must also have the RDRAM refreshed.

As to claim 17, the **Direct Rambus™ Technology Disclosure** teaches the refresh timing circuit further comprises:

a clock generator to generate the clock pulses (e.g., see the section titled **Clocking** on page 9);

a first counter coupled to the clock generator to count the number of clock pulses between memory refresh events is taught inherently as being a necessary element used for

refresh events, the memory must be refreshed on a periodic basis or time frame, this time frame must be detected or tracked and the method of doing this functionality is counting the clock pulses to determine the time since the last refresh event, the counter is incremented until a comparison with a predetermined number of clock pulses indicates a refresh must be performed (e.g., see the section titled **Clocking** on page 9 and the section titled **Features of the Rambus Memory Controller** on pages 14-15);

a storage register coupled to the clock generator and the counter to store a value representing the number of clock pulses between memory refresh events and a comparator coupled to the clock generator, the counter and the storage register as the memory controller clearly supporting the necessary refresh function required for dynamic random access memory, different types of DRAM or RDRAM have different time requirements for when the memory must be refreshed to maintain the data integrity, to perform the refresh function the memory controller must store the predetermined value indicating when the refresh must be performed, the memory controller compares the number of clock pulses which have occurred since the last refresh operation to the predetermined number of clock pulses, when these values match the refresh is executed, given the details of the reference, this is the method and elements which one of ordinary skill in the art would know to be the method and elements used in the refreshing of the reference (e.g., see the section titled **Features of the Rambus Memory Controller** on pages 14-15).

As to claim 18, the **Direct Rambus™ Technology Disclosure** teaches the refresh timing circuit triggers memory refresh events whenever the computer system is operating in a low power mode, the memory refresh events triggered based upon the evaluated time between memory refresh events when the computer is operating in a normal mode as a self-refresh

function which is used for low power applications (e.g., see the first paragraph of the second column on page 13).

As to claim 19, the **Direct Rambus™ Technology Disclosure** used as 35 USC §102(b) art is still applied as given in the previous rejection, (the final office action, paper # 13 and repeated in the examiner's answer, paper # 19), this rejection for this non-amended claim was affirmed by the Board of Patent Appeals and Interferences and is now applied *res judicata*.

10. The **Direct Rambus™ Technology Disclosure** teaches the invention (claim 38) as claimed including a refresh timing circuit comprising:

an internal clock generator (e.g., see the section titled **Clocking** on page 9) having:

a host clock refresh counter to reference a host clock signal to generate memory refresh events whenever a computer system is operating in a normal mode as the system using an external clock generator for the external clock signals as opposed to the internal clock generator (e.g., see Figure 4 on page 8); and,

a clock generator to generator clock signals to trigger the memory refresh events whenever the computer system is operating in a low power mode (e.g., see the section titled **DRAM Core Options** on pages 12-13, specifically the last paragraph of the section).

As to claim 39, the **Direct Rambus™ Technology Disclosure** teaches the refresh timing circuit further comprises:

a first counter coupled to the clock generator to count the number of clock pulses between memory refresh events is taught inherently as being a necessary element used for refresh events, the memory must be refreshed on a periodic basis or time frame, this time frame must be detected or tracked and the method of doing this functionality is counting the clock

pulses to determine the time since the last refresh event, the counter is incremented until a comparison with a predetermined number of clock pulses indicates a refresh must be performed (e.g., see the section titled **Clocking** on page 9 and the section titled **Features of the Rambus Memory Controller** on pages 14-15);

a storage register coupled to the clock generator and the counter to store a value representing the number of clock pulses between memory refresh events and a comparator coupled to the clock generator, the counter and the storage register as the memory controller clearly supporting the necessary refresh function required for dynamic random access memory, different types of DRAM or RDRAM have different time requirements for when the memory must be refreshed to maintain the data integrity, to perform the refresh function the memory controller must store the predetermined value indicating when the refresh must be performed, the memory controller compares the number of clock pulses which have occurred since the last refresh operation to the predetermined number of clock pulses, when these values match the refresh is executed, given the details of the reference, this is the method and elements which one of ordinary skill in the art would know to be the method and elements used in the refreshing of the reference (e.g., see the section titled **Features of the Rambus Memory Controller** on pages 14-15).

As to claim 40, the **Direct Rambus™ Technology Disclosure** used as 35 USC §102(b) art is still applied as given in the previous rejection, (the final office action, paper # 13 and repeated in the examiner's answer, paper # 19), this rejection for this non-amended claim was affirmed by the Board of Patent Appeals and Interferences and is now applied *res judicata*.

35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 6-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the **Direct Rambus™ Technology Disclosure.**

As to claims 6-14, the **Direct Rambus™ Technology Disclosure** used as 35 USC §103 art is still applied as given in the previous rejection, (the final office action, paper # 13 and repeated in the examiner's answer, paper # 19), this rejection for these non-amended claims was affirmed by the Board of Patent Appeals and Interferences and is now applied *res judicata*.

As to claims 20-28, the **Direct Rambus™ Technology Disclosure** used as 35 USC §103 art is still applied as given in the previous rejection, (the final office action, paper # 13 and repeated in the examiner's answer, paper # 19), this rejection for these non-amended claims was affirmed by the Board of Patent Appeals and Interferences and is now applied *res judicata*.

As to claims 41-49, the **Direct Rambus™ Technology Disclosure** used as 35 USC §103 art is still applied as given in the previous rejection, (the final office action, paper # 13 and repeated in the examiner's answer, paper # 19), this rejection for these non-amended claims was affirmed by the Board of Patent Appeals and Interferences and is now applied *res judicata*.

RELATED PRIOR ART

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Baweja, P/N 6,216,233, Baweja et al. P/N 6,212,599 and Mnich et al. P/N 5,262,998

both deal with refresh timing circuitry for system which utilize both a normal power mode of operation and a low power mode of operation.

CONCLUSION

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

August 17, 2005